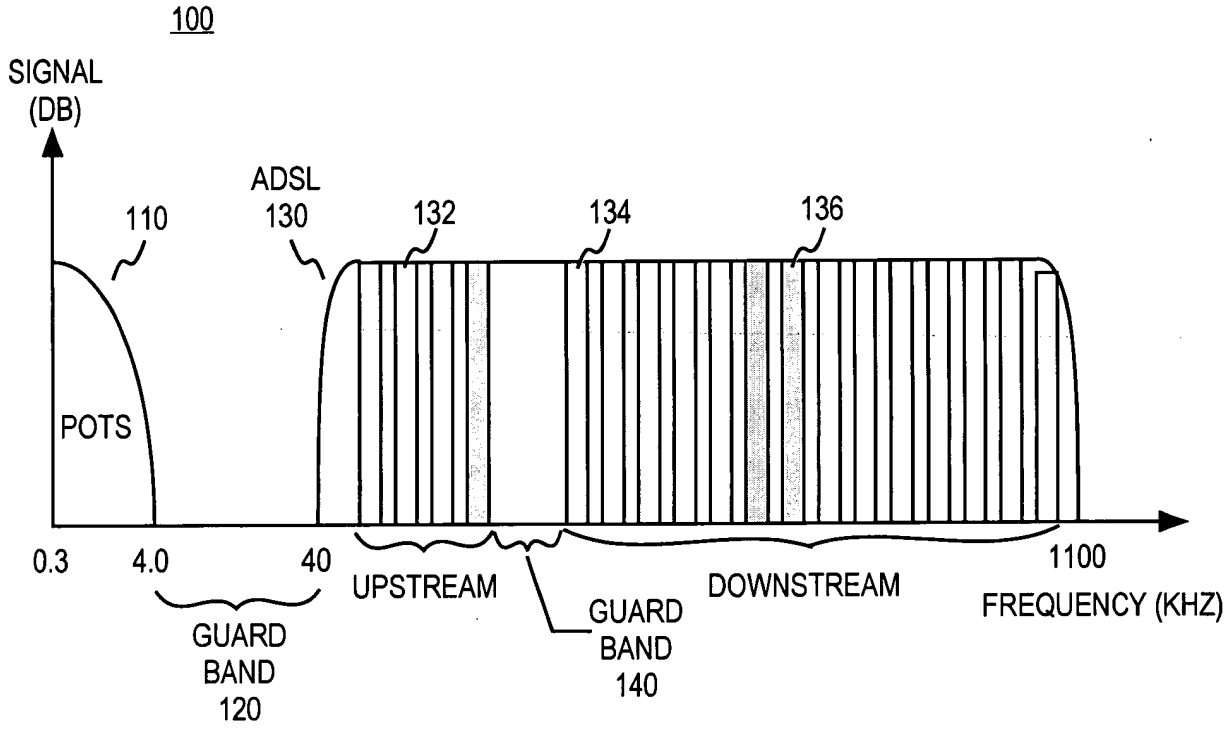

100
SIGNAL
(DB)
110
ADSL
130
132
134
136
POTS
0.3
4.0
40
UPSTREAM
GUARD
BAND
140
DOWNSTREAM
1100
FREQUENCY (KHZ)
GUARD
BAND
120

FIG. 1

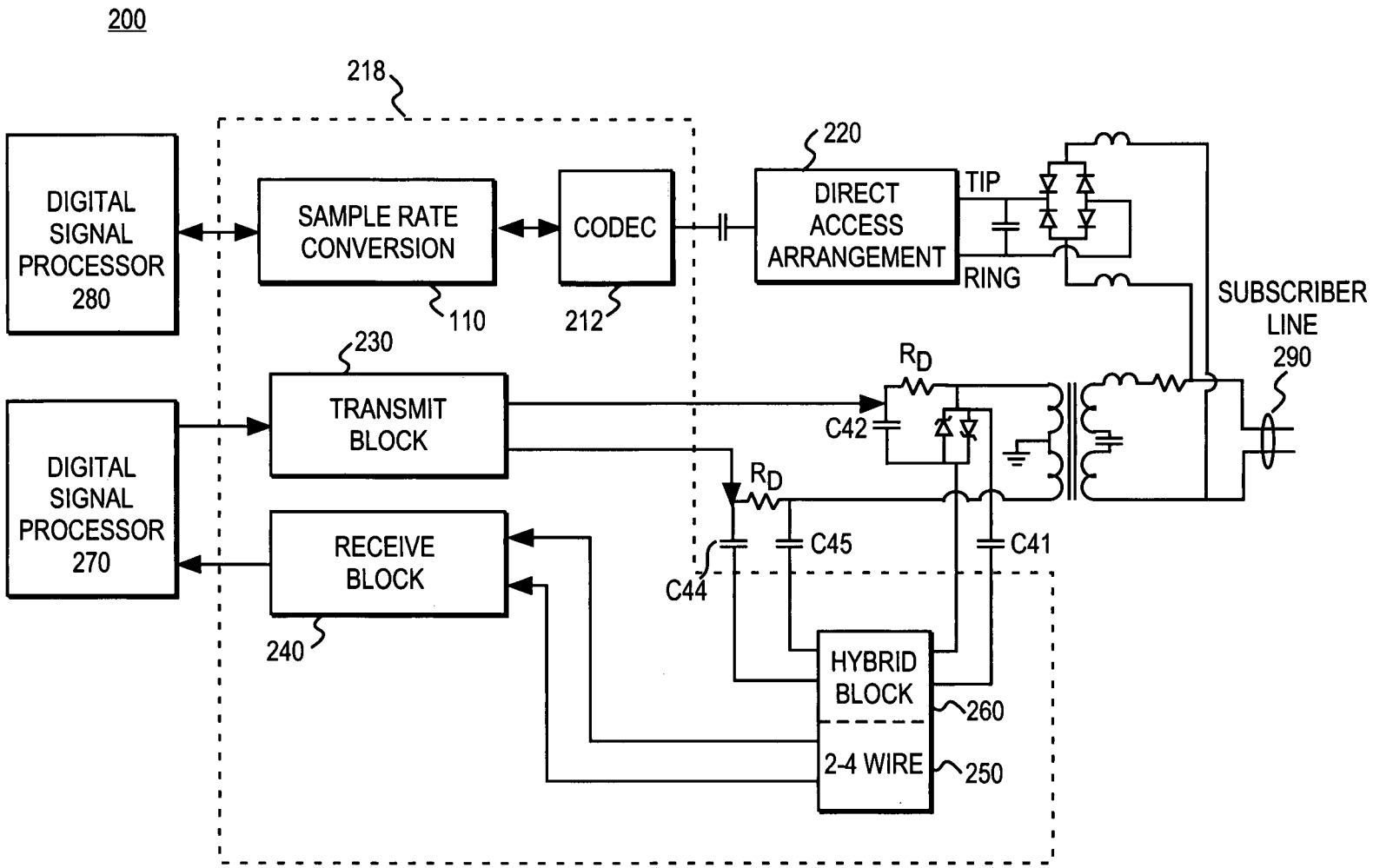
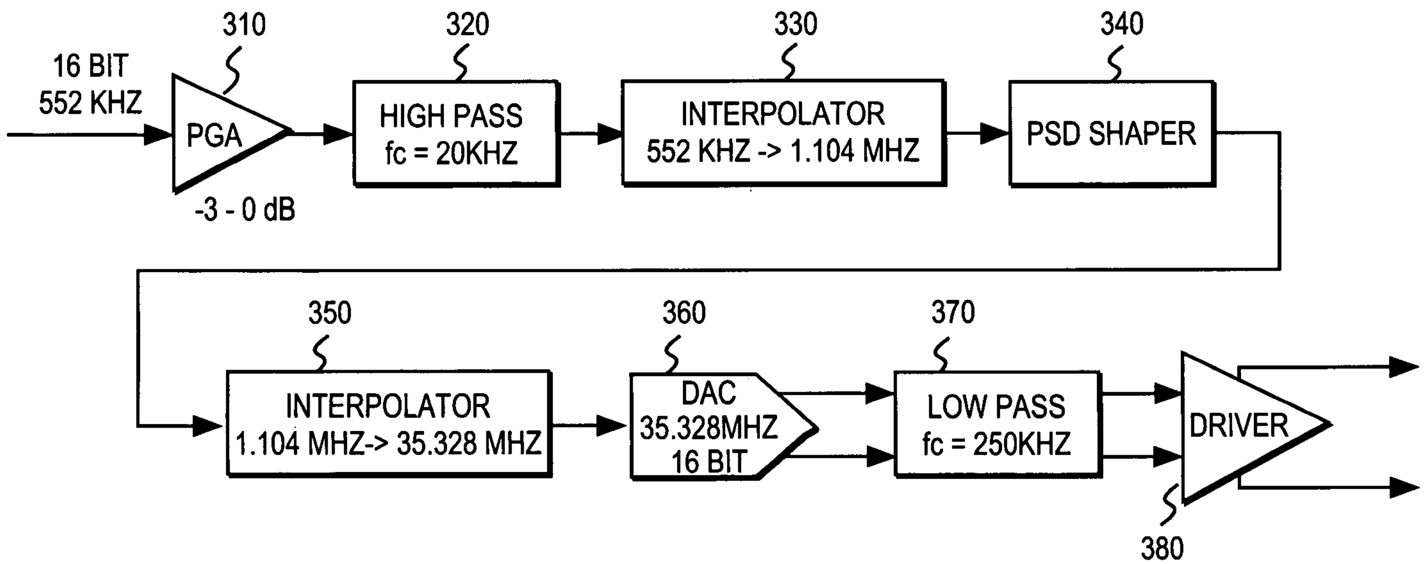

200
218
DIGITAL SIGNAL PROCESSOR 280
SAMPLE RATE CONVERSION
110
CODEC
212
220
DIRECT ACCESS ARRANGEMENT
TIP
RING
SUBSCRIBER LINE
290
230
TRANSMIT BLOCK
DIGITAL SIGNAL PROCESSOR 270
RECEIVE BLOCK
240
R_D
C42
R_D
C44
C45
C41
HYBRID BLOCK
260
2-4 WIRE
250

FIG. 2



16 BIT
552 KHZ
310
PGA
-3 - 0 dB
320
HIGH PASS
fc = 20KHZ
330
INTERPOLATOR
552 KHZ -> 1.104 MHZ
340
PSD SHAPER
350
INTERPOLATOR
1.104 MHZ-> 35.328 MHZ
360
DAC
35.328MHZ
16 BIT
370
LOW PASS
fc = 250KHZ
DRIVER
380

FIG. 3

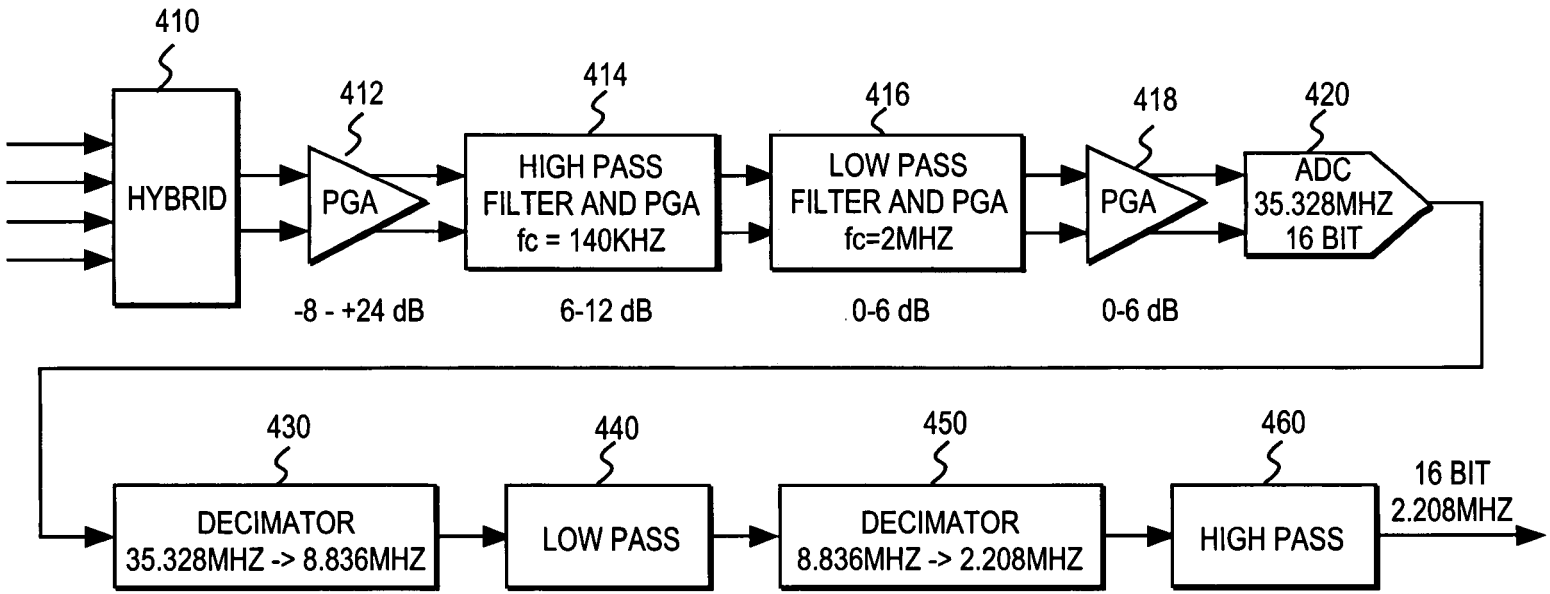

410
HYBRID
412
PGA
-8 - +24 dB
414
HIGH PASS
FILTER AND PGA
fc = 140KHZ
6-12 dB
416
LOW PASS
FILTER AND PGA
fc=2MHZ
0-6 dB
418
PGA
0-6 dB
420
ADC
35.328MHZ
16 BIT
430
DECIMATOR
35.328MHZ -> 8.836MHZ
440
LOW PASS
450
DECIMATOR
8.836MHZ -> 2.208MHZ
460
HIGH PASS
16 BIT
2.208MHZ

FIG. 4

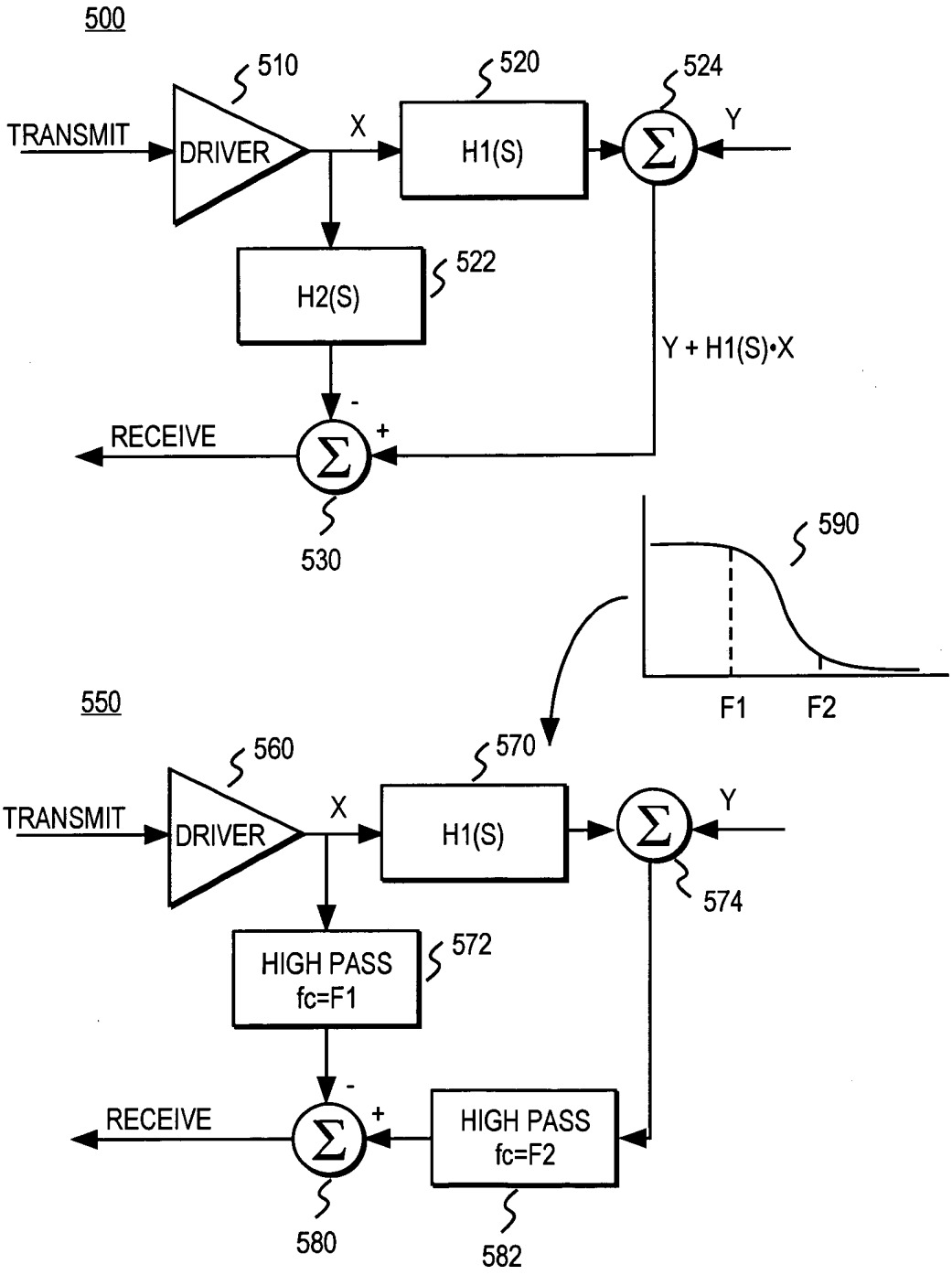

500
510
520
524
TRANSMIT
DRIVER
X
H1(S)
Y
H2(S)
522
Y + H1(S)•X
RECEIVE
530
590
F1
F2
550
560
570
TRANSMIT
DRIVER
X
H1(S)
Y
574
HIGH PASS
fc=F1
572
RECEIVE
HIGH PASS
fc=F2
580
582

FIG. 5

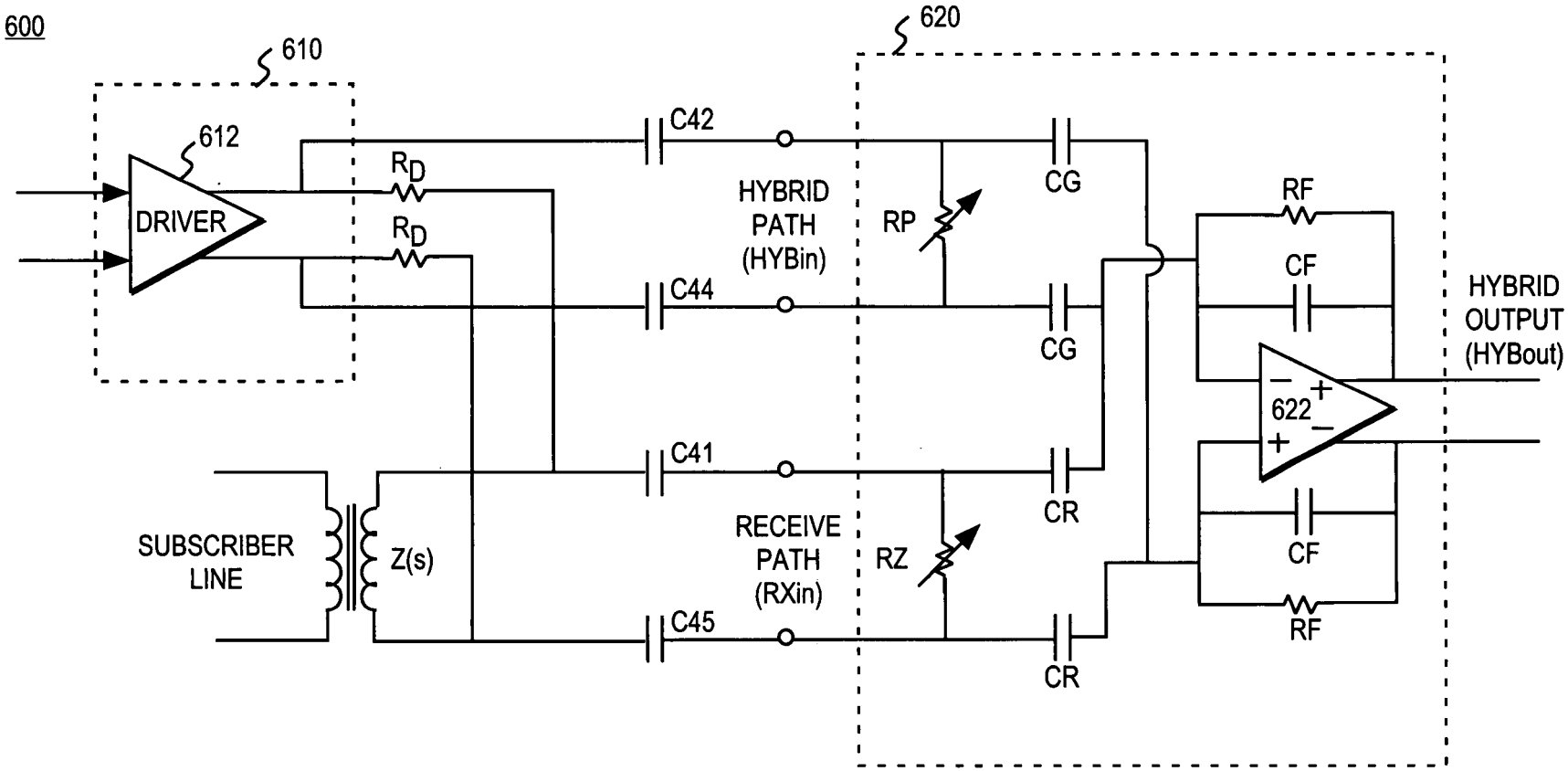

600
610
620
612
DRIVER
R_D
R_D
C42
C44
C41
C45
HYBRID
PATH
(HYBin)
RECEIVE
PATH
(RXin)
RP
RZ
CG
CG
CR
CR
RF
CF
CF
RF
622
HYBRID
OUTPUT
(HYBout)
SUBSCRIBER
LINE
Z(s)

FIG. 6

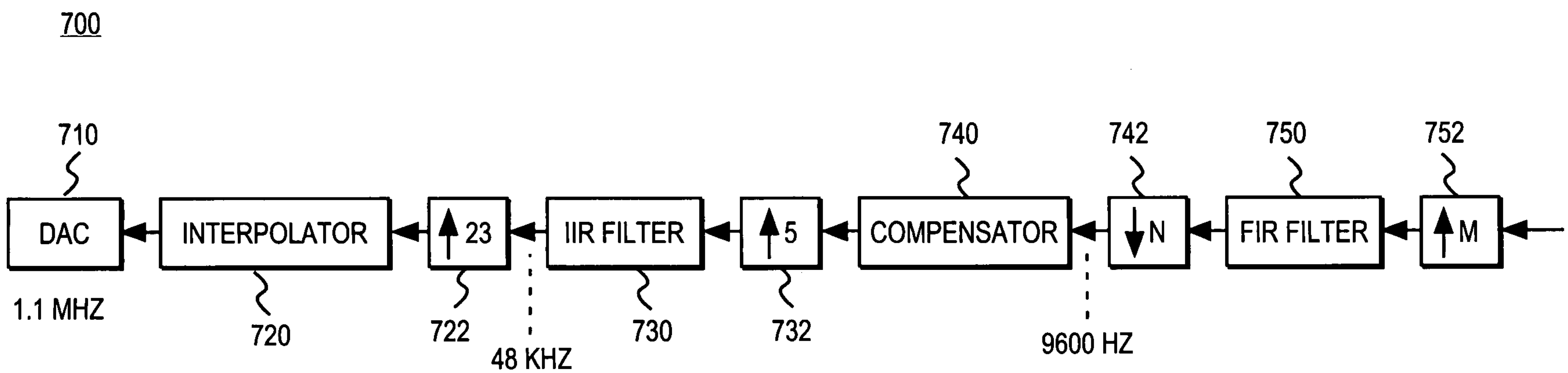

700
710
DAC
1.1 MHZ
INTERPOLATOR
720
23
722
48 KHZ
IIR FILTER
730
5
732
COMPENSATOR
740
9600 HZ
N
742
FIR FILTER
750
M
752

FIG. 7

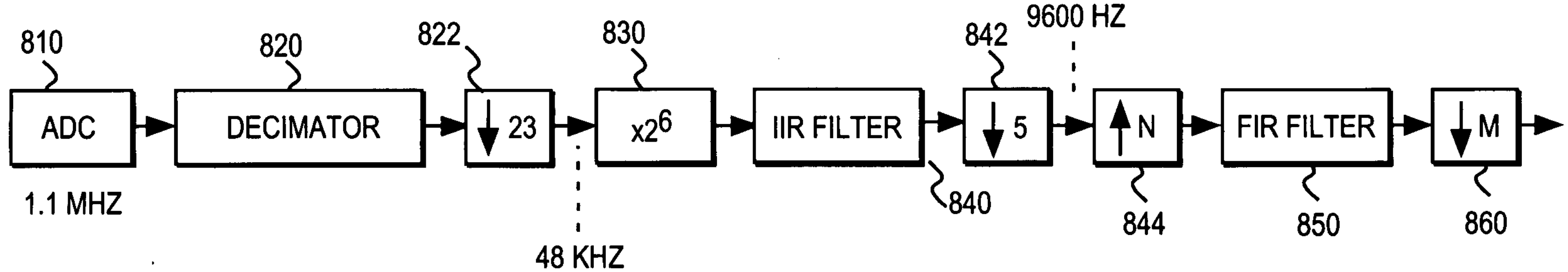

810
ADC
1.1 MHZ
820
DECIMATOR
822
23
48 KHZ
830
x2^6
IIR FILTER
840
842
5
9600 HZ
N
844
FIR FILTER
850
M
860

FIG. 8

900

	A->D			D->A	
f_i	M/N	OPT M/N	f_{audio}	N/M	N/M•f_{audio}
7200	8/6	16/12	9600	12/16	7200
8000	6/5	6/5	9600	5/6	8000
8229	7/6	14/12	9600	12/14	8228.57
8400	8/7	16/14	9600	14/16	8400
9000	16/15	16/15	9000	15/16	9000
9600	1/1	16/16	9600	16/16	9600
10,286	14/15	14/15	9600	15/14	10,285.71

FIG. 9

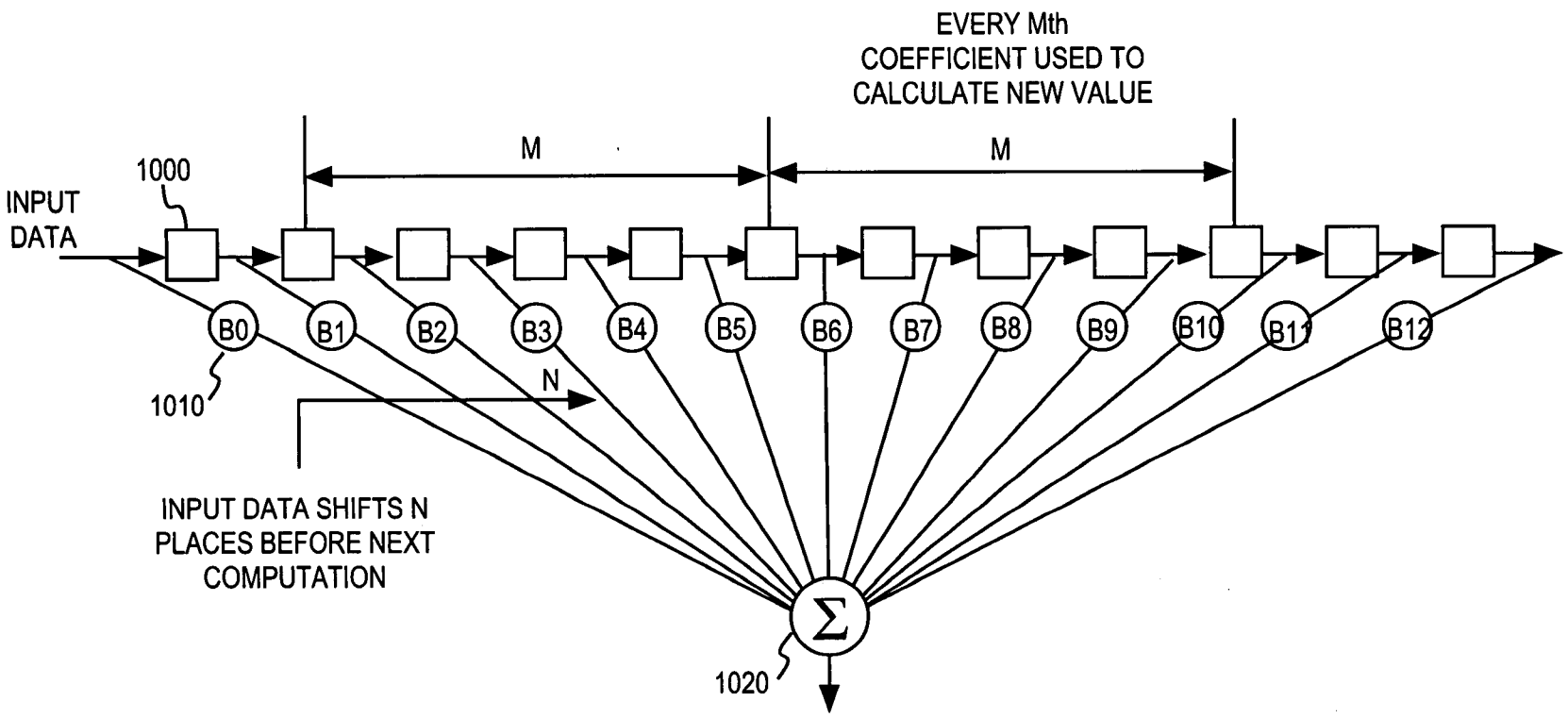

EVERY Mth
COEFFICIENT USED TO
CALCULATE NEW VALUE
M
M
1000
INPUT
DATA
B0
B1
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
B12
1010
N
INPUT DATA SHIFTS N
PLACES BEFORE NEXT
COMPUTATION
Σ
1020

FIG. 10

1100

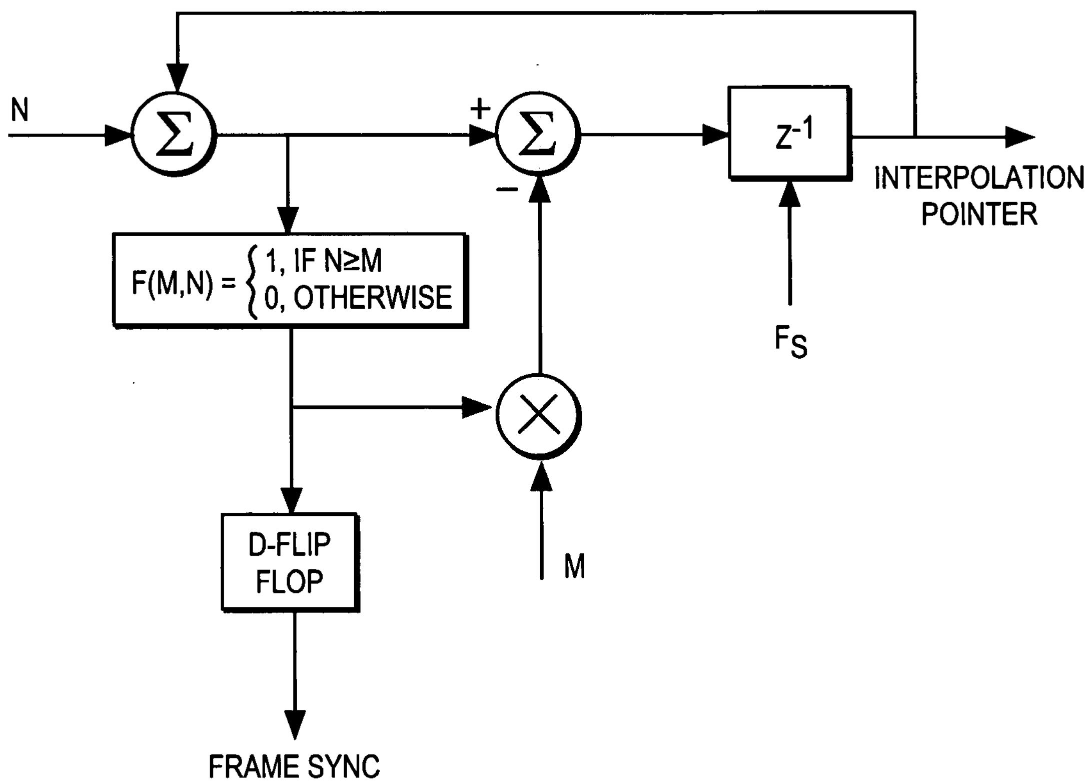

N
+
−
Σ
Σ
F(M,N) = { 1, IF N≥M
0, OTHERWISE
Z-1
INTERPOLATION
POINTER
FS
M
D-FLIP
FLOP
FRAME SYNC

FIG. 11

1200

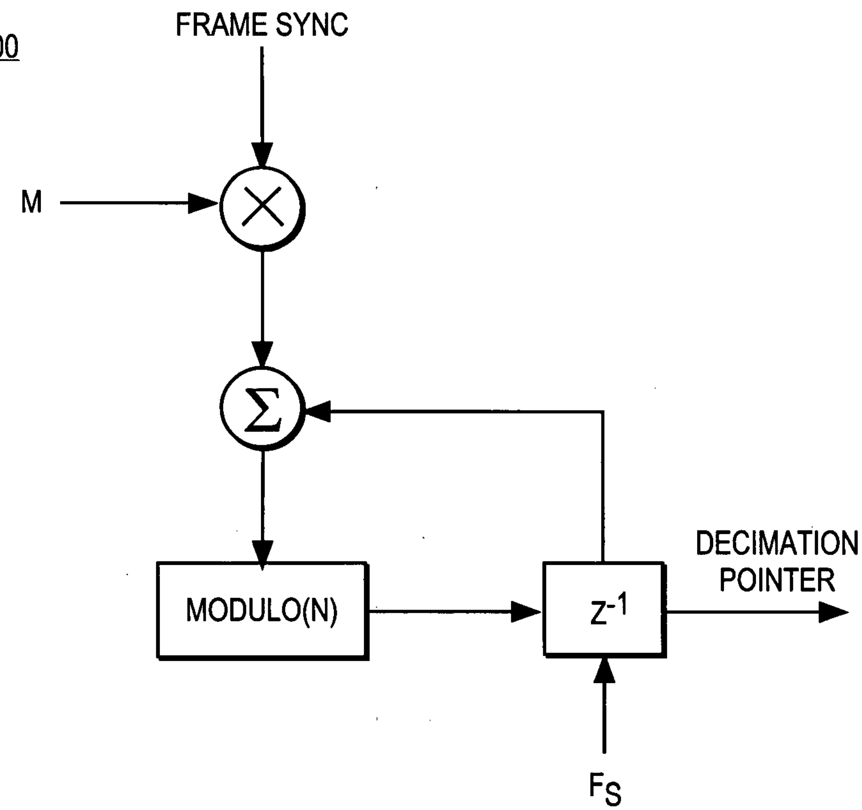


FIG. 12